REMARKS

In reply to the Office Action of March 10, 2005, Applicant submits the following remarks. Claims 21-26, 32 and 34-36 have been amended. Applicant respectfully requests reconsideration in view of the foregoing amendments and these remarks.

Objection to the Specification

The title was objected to as not being sufficiently descriptive. The title has been changed to Fabricating Surface Mountable Semiconductor Components with Leadframe Strips. The applicant believes this amendment addresses the Examiner's objection.

Section 112 Rejections

Claim 26 was rejected under 35 U.S.C. § 112 as being indefinite. The Examiner argues that "light generating epitaxial layers" is vague and indefinite because it is not clear where the layers are located in the semiconductor component. The applicant respectfully disagrees. There are no other components of the chip have been described in the claim and thus there is no possibility of confusion regarding the location of the light generating epitaxial layers.

Section 103 Rejections

Claims 21-24, 27 and 30-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over WO 94/11902 ("Kuraishi") in view of EP 1056126 ("Kobayashi"). The applicant respectfully disagrees.

Amended claims 21 and 23 are both directed to a method for producing a surface-mountable semiconductor component. Regarding claim 21, a semiconductor chip is mounted to a first side of a connection conductor through a chip window. An electrical contact of the semiconductor chip is electrically connected to a first side of a connector conductor. Regarding claim 23, a semiconductor chip is mounted so that first and second contacts of the semiconductor chip are electrically connected to first sides of connection conductors. Both claims 21 and 23 include mount a semiconductor chip that is capable of emitting and/or receiving electromagnetic

radiation and the claims include a step of encapsulating, where subsequent to encapsulation, the side opposite to the first side of the connector conductors are exposed for electrical connection to an electrical component.

Kuraishi describes an inner lead bonding-type semiconductor device having a semiconductor chip 24 mounted on an inner lead 18 (Fig. 6A, page 9, lines 20-30, page 11, lines 10-30). A mold resin 26 covers the semiconductor chip 24 and a backside of the inner lead 18. The inner lead 18 extends out to an outer lead 20. The resin enclosed semiconductor chip 24 can be electrically connected to a printed circuit board by way of the outer lead 20 (page 10, lines 9-23).

Kobayashi describes a device having a transistor 14b mounted on an electrode 11a (Figs. 2A-2C, paragraph 0053-0059). The electrode 11a connected to the transistor 14a is formed on one side of a ceramic substrate 32. A lower electrode 22a is in electrical communication with the upper electrode 11a through a via 17a in the ceramic 32 filled with electrically conductive paste. The transistor 14 is coated and sealed with a coating resin for transfer molding, such that the ceramic is not coated (paragraph 0034).

Both Kuraishi and Kobayashi fail to describe a device having a semiconductor chip capable of emitting and/or receiving electromagnetic radiation. Kuraishi only describes mounting a semiconductor chip on a lead. Kobayashi describes mounting transistors rather than a semiconductor chip capable of emitting and/or receiving electromagnetic radiation. Both Kuraishi and Kobayashi fail to describe a device where subsequent to the encapsulation step, the connection conductors on a side opposite to the first side are exposed for electrical connection to an electrical component. Kuraishi encapsulates both sides of the inner lead 18 and Kobyashi has a ceramic layer or a conductive paste covering the electrode 11a.

Additionally, the device described by Kuraishi could not be encapsulated with the method described by Kobayashi. The transfer molding process described by Kobayashi exposes the structure to be molded to considerable mechanical loading due to the compression step during the molding process. The base film 10 and inner leads 18 of Kuraishi's device are very sensitive to mechanical loading because of their thin nature. For at least these reasons, the

applicant submits that no *prima facie* case of obviousness has been made with respect to claims 21 and 23. Claims 22, 24, 27 and 30-32 depend from at least one of claims 21 and 23 and are not obvious over the combination of Kuraishi and Kobayashi for at least the same reasons.

Claims 25, 28 and 29 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuraishi and Kobayashi in view of U.S. Patent No. 6,486,543 ("Sano"). Claims 33-40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuraishi and Kobayashi in view of U.S. Patent No. 6,586,323 ("Fan"). The applicant respectfully disagrees.

Each of claims 25, 28, 29 and 33-40 depend from at least one of claims 21 or 23 and necessarily include the limitations of claims from which they depend.

Sano describes a resin-packaged semiconductor device where the semiconductor device 3, such as an LED, contacts a first side of terminals 11 and a resin package 4 contacts the opposite side of the terminals (Fig. 1, col. 6, lines 23-48).

Fan describes an under bump metallurgy layer 18 sandwiched between a solder bump 20 and a contact pad 12 (Fig. 2, col. 3, lines 1-14). The other side of the contact pad 12 is covered by a semiconductor substrate 10.

Both Sano and Fan fail to suggest or disclose that subsequent to an encapsulation step, the connection conductors on a side opposite to the first side, where the first side is the side on which a semiconductor device has been mounted, are exposed for electrical connection to an electrical component. Further, with respect to Sano, the Examiner has provided no motivation for why a person of ordinary skill in the art would put the LED of Sano into the packaging described by Kuriashi or Kobayashi. For at least these reasons, the applicant submits that no *prima facie* case of obviousness has been made with respect to claims 25, 28, 29 and 33-40.

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Please apply the One-Month Extension of Time fee in the amount of $120 and any other appropriate charges or credits to deposit account 06-1050.

Respectfully submitted,

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